PIxEQX6741Sx

PIxEQX6741Sx SATA ReDriver Application Information
Feb. 18, 2011

Contents

General Introduction

PIxEQX6741Sx SATA ReDriver^{TM} are developed to redrive one full lane of SAS/SATA up to 6Gbps signal, it have lower power consumption and excellent performance.

The parts include PI3EQX6741STZDE, PI3EQX6741STBZDE and PI2EQX6741SLZDE. And PI2EQX6741SLZDE operates from +1.05V power supply, the other two parts operates from +3.3V power supply.

External Components Requirement

PIxEQX6741SxZDE requires AC coupling capacitors for all redriver inputs and outputs. High-quality, low-ESR, X7R, 10nF, 0402-sized capacitors are recommended.

Layout Design Guide

■ **Layout Considerations for Differential Pairs**
   ✓ The trace length miss-matching shall be less than 5 mils for the "+" and "–" traces in the same pairs
   ✓ Use wider trace width, with 100ohm differential impedance, to minimize the loss for long routes
   ✓ Target differential Zo of 100ohm ±20%
   ✓ More pair-to-pair spacing for minimal crosstalk coupling, it is recommended to have >3X gap spacing between differential pairs.
   ✓ It is preferable to route differential lines exclusively on one layer of the board, particularly for the input traces
   ✓ The use of vias should be avoided if possible, if vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair.
   ✓ Route the differential signals away from other signals and noise sources on the printed circuit board
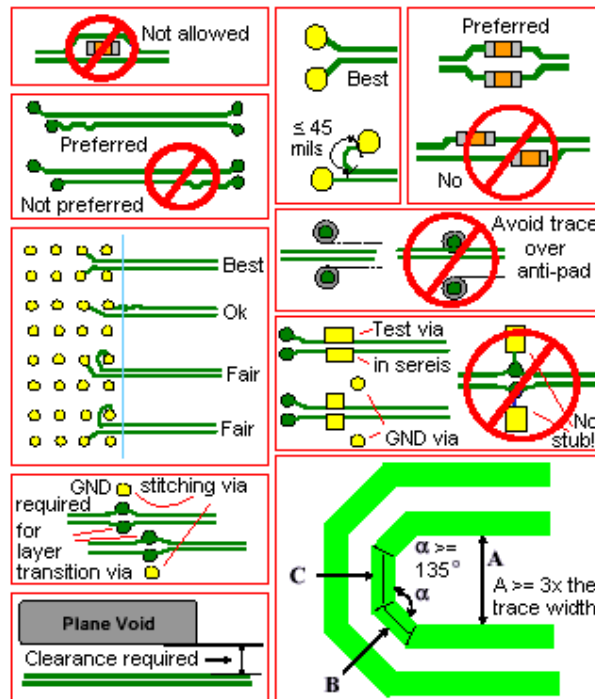
■ **PCB Layout Trace Routings**

Figure1 Layout Sample for Trace Routings

Power-Supply bypass

More careful attention must be paid to the details associated with high-speed design as well as providing a clean power supply; there are some approaches as recommendation.

✓ The supply (VDD) and ground (GND) pins should be connected to power planes routed on adjacent layers of the printed circuit board. The distance to plane should be <50mil.
✓ The layer thickness of the dielectric should be minimized so that the VDD and GND planes create a low inductance supply with distributed capacitance.
✓ Careful attention to supply bypassing through the proper use of bypass capacitors is required. A low-ESR 0.01uF bypass capacitor should be connected to each VDD pin such that the capacitor is placed as close as possible to PIxEQX6741SxZDE. Smaller body size capacitors can help facilitate proper component placement. The distance of capacitors to IC body should be <100mil.
✓ One capacitor with capacitance in the range of 1uF to 10uF should be incorporated in the power supply bypassing design as well. It is can be either tantalum or an ultra-low ESR ceramic.

Power Supply Sequencing

Proper power supply sequencing is recommened for all devices. Always apply GND and VDD before applying signals., especially if the signal is not current limited.

Caution: Do NOT exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the device.

Equalization and Pre-emphasis Setting

■ **Various Input Trace and Eye Test with different EQ setting**

Figure2 is PIxEQX6741SxZDE test setup for different EQ setting, R is PIxEQX6741SxZDE.
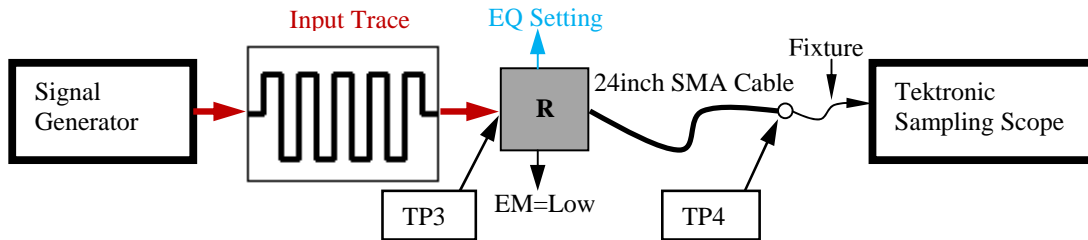Signal Source: PRBS2^7-1 pattern, Differential Voltage is 600mV, Pre-emphasis is 0dB

Figure2 PIxEQX6741SxZDE test setup for different EQ setting

Table1 Eye Diagram vs. Input FR4 trace and EQ setting at 6Gb/s

Input Trace Length	EQ Setting	Input Eye at TP3	Output Eye at TP4
6 inch FR4 Lab trace (-2dB loss at 3GHz)	3dB (A_EQ or B_EQ =Low)		
18 inch FR4 Lab trace (-6dB loss at 3GHz)	3dB (A_EQ or B_EQ =Low)		
30 inch FR4 Lab trace (-10dB at 3GHz)	6dB (A_EQ or B_EQ =Open)		
48 inch FR4 Lab trace (-16dB loss at 3GHz)	9dB (A_EQ or B_EQ =High)		

Table2 Eye Diagram vs. Input FR4 trace and EQ setting at 3Gb/s

Input Trace Length	EQ Setting	Input Eye at TP3	Output Eye at TP4
6 inch FR4 Lab trace (-1.2dB loss at 1.5GHz)	2.5dB (A_EQ or B_EQ =Low)		
18 inch FR4 Lab trace (-3dB loss at 1.5GHz)	2.5dB (A_EQ or B_EQ =Low)		
30 inch FR4 Lab trace (-5dB loss at 1.5GHz)	5dB (A_EQ or B_EQ =Open)		
48 inch FR4 Lab trace (-9dB loss at 1.5GHz)	7.5dB (A_EQ or B_EQ =High)		

■ **Various Output Trace and Eye Test with different pre-emphasis setting**

Figure2 is PIxEQX6741SxZDE test setup for different EM setting, R is PIxEQX6741SxZDE.
Signal Source: PRBS2^7-1 pattern, Differential Voltage is 600mV, Equalization is 0dB
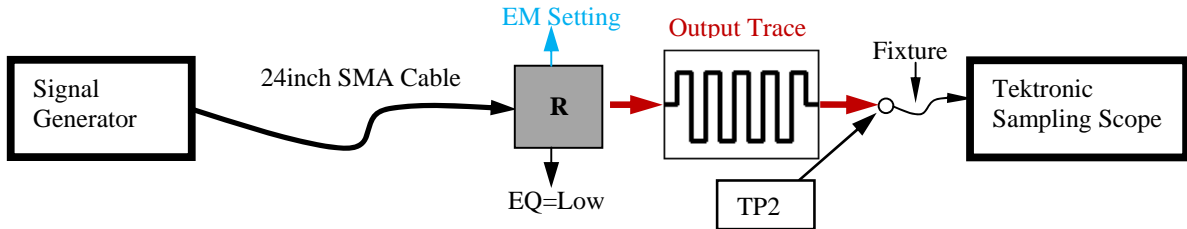

Figure2 PIxEQX6741SxZDE test setup for different EM setting

Table3 Eye Diagram vs. Output FR4 Trace and EM setting at 6Gb/s

EM Setting	Eye Test at TP2 for Various Output Trace		
	No trace	6 inch FR4 Lab trace (-2dB loss at 3GHz)	12 inch FR4 Lab trace (-4dB loss at 3GHz)
EM=low			
EM=High			

Table4 Eye Diagram vs. Output FR4 Trace and EM setting at 3Gb/s

EM Setting	Eye at TP2 for Various Output Trace		
	No trace	6 inch FR4 Lab trace (-1.2dB loss at 1.5GHz)	12 inch FR4 Lab trace (-2.2dB loss at 1.5GHz)
EM=low			
EM=High			

Typical application circuit

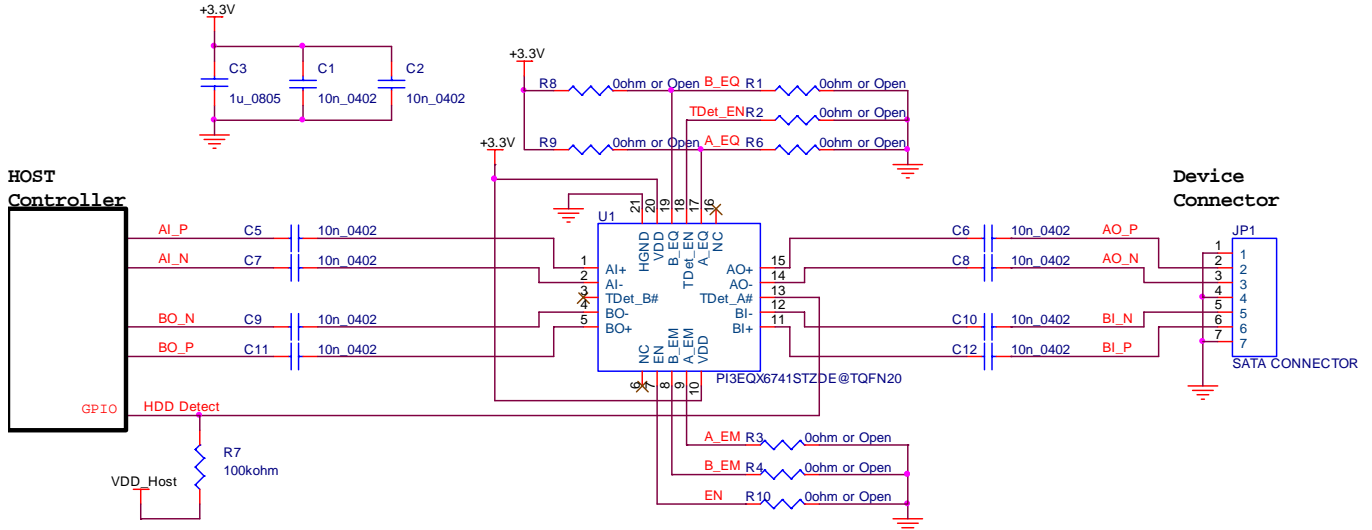Figure3 shows typical application circuit of PI3EQX6741STZDE.

Figure3 Typical Application Circuit of PI3EQX6741STZDE

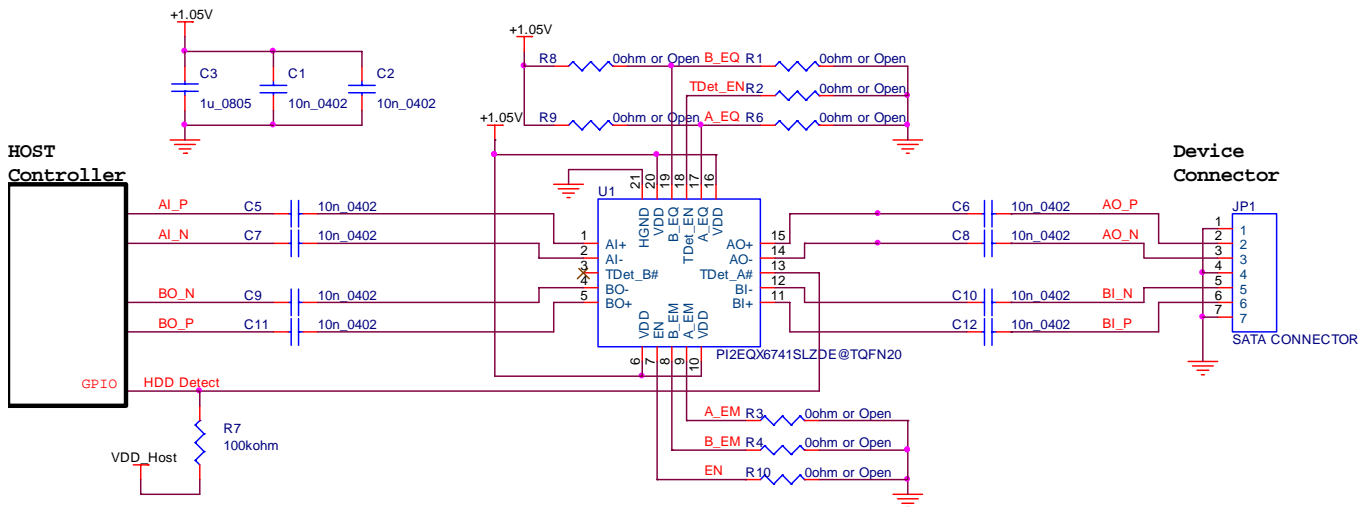Figure4 shows typical application circuit of PI2EQX6741SLZDE.

Figure4 Typical Application Circuit of PI2EQX6741SLZDE

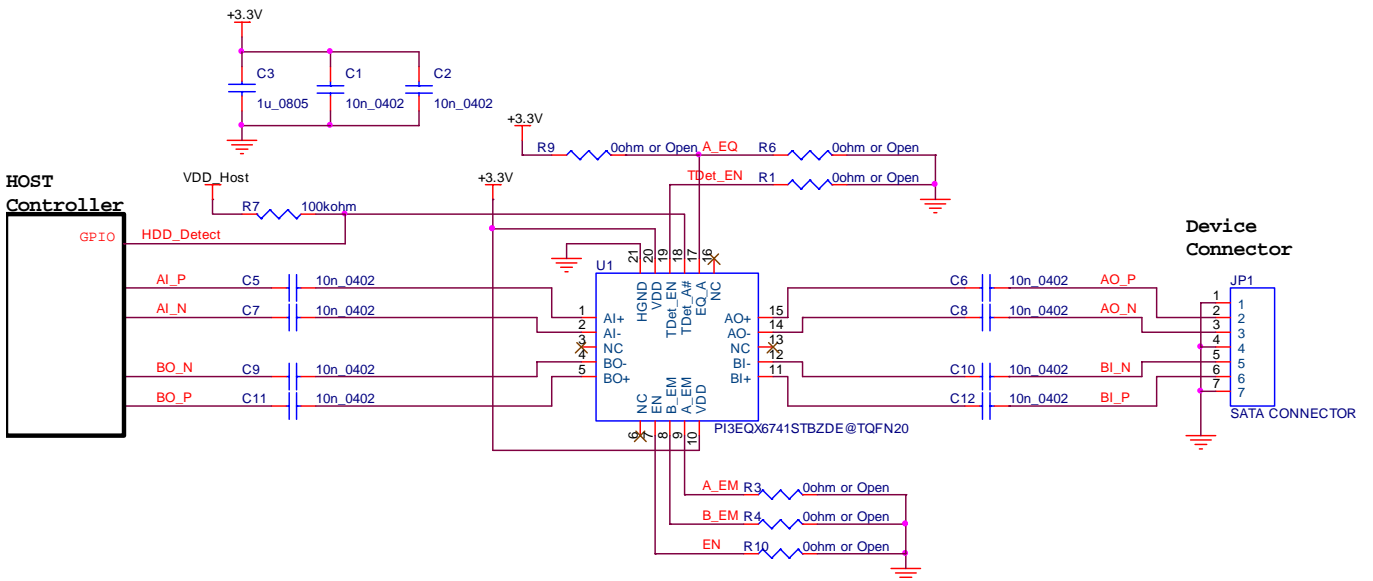Figure5 shows typical application circuit of PI3EQX6741STBZDE.

Figure5 Typical Application Circuit of PI3EQX6741STBZDE

PCB Layout Sample

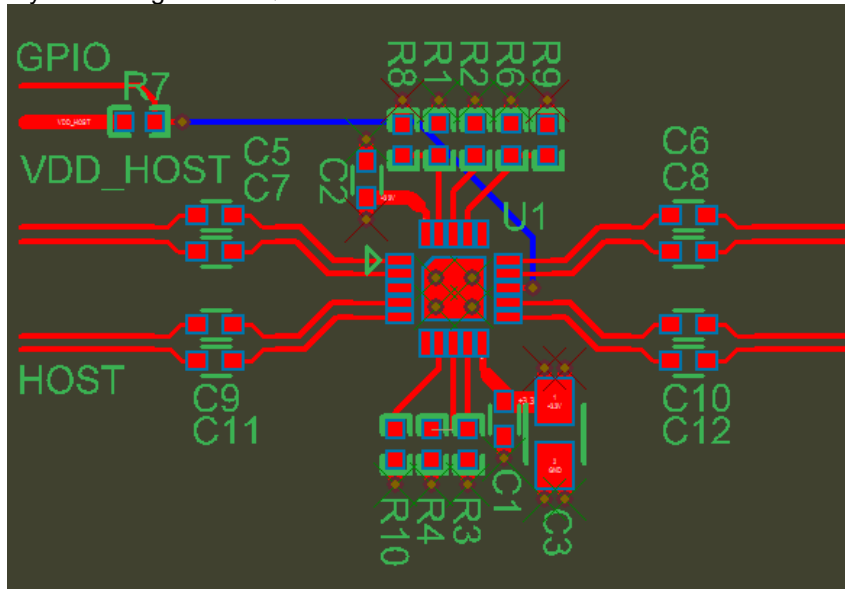Figure6 shows typical layout routing of PI3EQX6741STZDE.

Figure6 Typical Layout Routing of PI3EQX6741STZDE

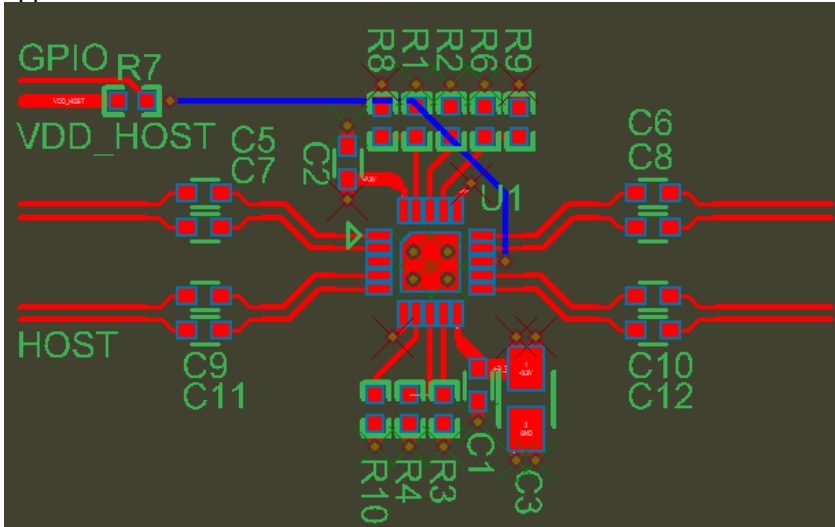Figure7 shows typical application circuit of PI3EQX6741SLZDE.

Figure7 Typical Layout Routing of PI3EQX6741SLZDE

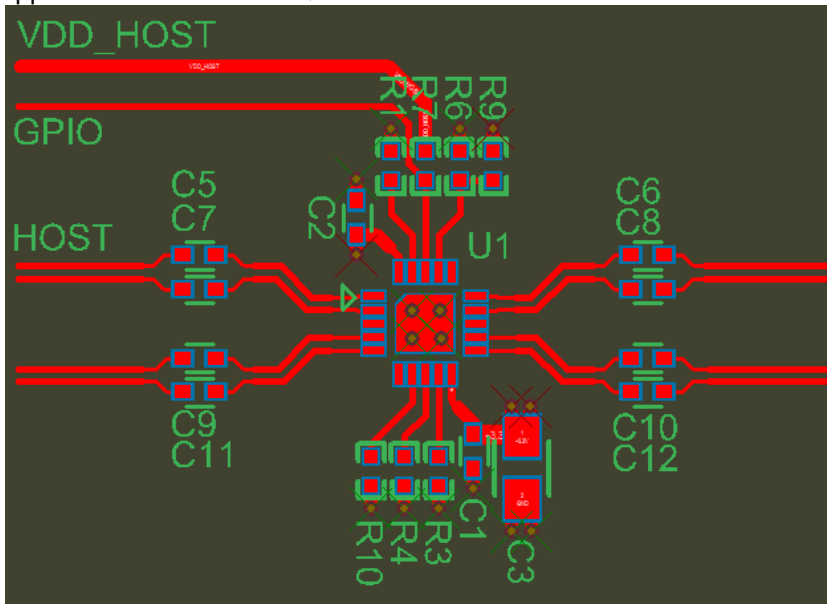Figure8 shows typical application circuit of PI3EQX6741STBZDE.

Figure8 Typical Layout Routing of PI3EQX6741STBZDE

History

Version 1.0   Original Version   Feb. 18, 2011